

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO.  <b>TI-34032A</b>		SERIAL NO.  <del>TDD</del> <b>10/761679</b>	
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>								
					APPLICANT: <b>Chiu et al.</b>			
					FILING DATE <del>Herewith</del> <b>01/20/04</b>		GROUP <b>2831 TDD</b>	
U.S. PATENT DOCUMENTS								
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)	
CO		US 6,385,049 B1	05/07/02	Chia-Yu et al.	361	721	07/05/2001	
CO		5,879,792	03/09/99	Watanabe et al.	428	304.4	01/13/1997	
CO		5,709,146	01/20/98	Watanabe	101	128.21	03/29/1996	
CO		US 6,213,347 B1	04/10/01	Thomas	222	52	04/30/1999	
CO		US 6,228,680 B1	05/08/01	Thomas	438	108	05/01/1999	
CO		US 6,245,583	06/12/01	Amador et al.	438	14	04/30/1999	
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SU B C L A S S	TRANSLATION	
							YES	NO
OTHER NON-PATENT DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>								
CO		"Flip-Chip On Film Assembly for Ball Grid Array Packages" Coyle et al., U. S. Patent Publication No. US 2002/0084521 A1, Published 4 July 2002						
CO		"Flexible Ball Grid Array Chip Scale Packages and Methods of Fabrication", Moon et al. U. S. Patent Publication No. US 2002/0164838 A1, Published 7 Nov., 2002						
CO		"Plastic Chip-Scale Package Having Integrated Passive Components", Pritchett et al., U. S. Patent Publication No. US 2002/0015292 A1, Published 7 Feb., 2002						
CO		"SLT Device Metallurgy and its Monolithic Extension", Totta et al., IBM J. Res. Develop. May, 1969, pp. 226-238						
CO		"Controlled Collapse Reflow Chip Joining", Miller, IBM Components Division, Fishkill New York, May 1969, pp. 239-250						
CO		"Geometric Optimization of Controlled Collapse Interconnections", Goldmann, IBM Components Division, Fishkill, New York, May 1969, pp. 251-265						
CO		"Reliability of Controlled Collapse Interconnections", Norris et al., IBM J. Res. Develop. May 1969, pp. 266-271						
CO		"Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Oktay, IBM J. Res. Develop., May 1969, pp. 272-285						
CO		"Studies of the SLT Chip Terminal Metallurgy", Berry et al, IBM J. Res. Develop. May 1969, pp. 286-296						
CO		"Parallel Methods for Approximating the Root of a Function", Miranker, IBM Watson Research Center, Yorktown Heights, New York, May 1969 pp. 297						
CO		"Chip Scale Package (CSP)", Lau et al, McGraw Hill						
CO		"Effect of Simulation Methodology on Solder Joint Crack Growth Correlation", Darveaux, IEEE Electronic Components and Technology Conference, 2000, pp. 1048-1058						
CO		"Reliability of Plastic Ball Grid Array Assembly, Darveaux, et al, Chapter 13						
EXAMINER  <i>Cal Shi</i>					DATE CONSIDERED  <b>10/30/04</b>			
<small>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>								